IFW AF/2827

PTO/SB/21 (03-03)
Approved for use through 04/30/2003. OMB 0651-0031
U.S. Patent and Trademark Office; U.S. DEPARTMENT OF COMMERCE


# TRANSMITTAL FORM

*(to be used for all correspondence after initial filing)*

| | |
|---|---|
| Application Number | 10/051,886 |
| Filing Date | April 6, 2001 |
| First Named Inventor | Valery Felmetsger |
| Art Unit | 2827 |
| Examiner Name | Alonzo Chambliss |
| Attorney Docket Number | SPUTT-57354 |

Total Number of Pages in This Submission

## ENCLOSURES *(Check all that apply)*

- [x] Fee Transmittal Form
  - [x] Fee Attached
- [ ] Amendment/Reply
  - [ ] After Final
  - [ ] Affidavits/declaration(s)
- [ ] Extension of Time Request
- [ ] Express Abandonment Request
- [ ] Information Disclosure Statement
- [ ] Certified Copy of Priority Document(s)
- [ ] Response to Missing Parts/ Incomplete Application
  - [ ] Response to Missing Parts under 37 CFR 1.52 or 1.53
- [ ] Drawing(s)
- [ ] Licensing-related Papers
- [ ] Petition
- [ ] Petition to Convert to a Provisional Application
- [ ] Power of Attorney, Revocation
- [ ] Change of Correspondence Address
- [ ] Terminal Disclaimer
- [ ] Request for Refund
- [ ] CD, Number of CD(s) _____
- [ ] After Allowance Communication to a Technology Center (TC)
- [ ] Appeal Communication to Board of Appeals and Interferences
- [x] Appeal Communication to TC **(Appeal Notice, Brief, Reply Brief)**
- [ ] Proprietary Information
- [ ] Status Letter
- [x] Other Enclosure(s) (please Identify below):

POSTCARD

Remarks

## SIGNATURE OF APPLICANT, ATTORNEY, OR AGENT

| | |
|---|---|
| Firm or Individual | FULWIDER PATTON LEE & UTECHT, LLP<br>ELLSWORTH R. ROSTON, ESQ., REG. NO. 16,310 |
| Signature | Ellsworth R. Roston |
| Date | August 5, 2004 |

## CERTIFICATE OF TRANSMISSION/MAILING

I hereby certify that this correspondence is being facsimile transmitted to the USPTO or deposited with the United States Postal Service with sufficient postage as first class mail in an envelope addressed to: Commissioner for Patents, Washington, DC 20231 on this date: 08/05/04

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|---|---|---|---|
| Typed or printed | ELLSWORTH R. ROSTON, REG. NO. 16,310 | | |
| Signature | Ellsworth R. Roston | Date | 08/05/04 |

PTO/SB/17 (10-03)
Approved for use through 07/31/2006. OMB 0651-0032
U.S. Patent and Trademark Office; U.S. DEPARTMENT OF COMMERCE


# FEE TRANSMITTAL for FY 2004

*Effective 10/01/2003. Patent fees are subject to annual revision.*

☑ Applicant claims small entity status. See 37 CFR 1.27

**TOTAL AMOUNT OF PAYMENT** ($) 165.00

| *Complete if Known* | |
|---|---|
| Application Number | 10/051,886 |
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| Attorney Docket No. | SPUTT-57354 |

## METHOD OF PAYMENT *(check all that apply)*

☑ Check ☐ Credit card ☐ Money Order ☐ Other ☐ None

☑ Deposit Account:

Deposit Account Number: 06-2425

Deposit Account Name: FULWIDER PATTON, et al.

**The Director is authorized to:** *(check all that apply)*

☐ Charge fee(s) indicated below ☐ Credit any overpayments

☑ Charge any additional fee(s) or any underpayment of fee(s)

☐ Charge fee(s) indicated below, **except for the filing fee** to the above-identified deposit account.

## FEE CALCULATION

### 1. BASIC FILING FEE

| Large Entity Fee Code | Large Entity Fee ($) | Small Entity Fee Code | Small Entity Fee ($) | Fee Description | Fee Paid |
|---|---|---|---|---|---|
| 1001 | 770 | 2001 | 385 | Utility filing fee | |
| 1002 | 340 | 2002 | 170 | Design filing fee | |
| 1003 | 530 | 2003 | 265 | Plant filing fee | |
| 1004 | 770 | 2004 | 385 | Reissue filing fee | |
| 1005 | 160 | 2005 | 80 | Provisional filing fee | |

SUBTOTAL (1) ($)

### 2. EXTRA CLAIM FEES FOR UTILITY AND REISSUE

| | Extra Claims | | Fee from below | | Fee Paid |
|---|---|---|---|---|---|
| Total Claims | | -20** = | | X | = |
| Independent Claims | | - 3** = | | X | = |
| Multiple Dependent | | | | | = |

| Large Entity Fee Code | Large Entity Fee ($) | Small Entity Fee Code | Small Entity Fee ($) | Fee Description |
|---|---|---|---|---|
| 1202 | 18 | 2202 | 9 | Claims in excess of 20 |
| 1201 | 86 | 2201 | 43 | Independent claims in excess of 3 |
| 1203 | 290 | 2203 | 145 | Multiple dependent claim, if not paid |
| 1204 | 86 | 2204 | 43 | ** Reissue independent claims over original patent |
| 1205 | 18 | 2205 | 9 | ** Reissue claims in excess of 20 and over original patent |

SUBTOTAL (2) ($)

**or number previously paid, if greater; For Reissues, see above

## FEE CALCULATION (continued)

### 3. ADDITIONAL FEES

| Large Entity Fee Code | Large Entity Fee ($) | Small Entity Fee Code | Small Entity Fee ($) | Fee Description | Fee Paid |
|---|---|---|---|---|---|
| 1051 | 130 | 2051 | 65 | Surcharge - late filing fee or oath | |
| 1052 | 50 | 2052 | 25 | Surcharge - late provisional filing fee or cover sheet | |
| 1053 | 130 | 1053 | 130 | Non-English specification | |
| 1812 | 2,520 | 1812 | 2,520 | For filing a request for *ex parte* reexamination | |
| 1804 | 920* | 1804 | 920* | Requesting publication of SIR prior to Examiner action | |
| 1805 | 1,840* | 1805 | 1,840* | Requesting publication of SIR after Examiner action | |
| 1251 | 110 | 2251 | 55 | Extension for reply within first month | |
| 1252 | 420 | 2252 | 210 | Extension for reply within second month | |
| 1253 | 950 | 2253 | 475 | Extension for reply within third month | |
| 1254 | 1,480 | 2254 | 740 | Extension for reply within fourth month | |
| 1255 | 2,010 | 2255 | 1,005 | Extension for reply within fifth month | |
| 1401 | 330 | 2401 | 165 | Notice of Appeal | |
| 1402 | 330 | 2402 | 165 | Filing a brief in support of an appeal | 165.00 |
| 1403 | 290 | 2403 | 145 | Request for oral hearing | |
| 1451 | 1,510 | 1451 | 1,510 | Petition to institute a public use proceeding | |
| 1452 | 110 | 2452 | 55 | Petition to revive - unavoidable | |
| 1453 | 1,330 | 2453 | 665 | Petition to revive - unintentional | |
| 1501 | 1,330 | 2501 | 665 | Utility issue fee (or reissue) | |
| 1502 | 480 | 2502 | 240 | Design issue fee | |
| 1503 | 640 | 2503 | 320 | Plant issue fee | |
| 1460 | 130 | 1460 | 130 | Petitions to the Commissioner | |
| 1807 | 50 | 1807 | 50 | Processing fee under 37 CFR 1.17(q) | |
| 1806 | 180 | 1806 | 180 | Submission of Information Disclosure Stmt | |
| 8021 | 40 | 8021 | 40 | Recording each patent assignment per property (times number of properties) | |
| 1809 | 770 | 2809 | 385 | Filing a submission after final rejection (37 CFR 1.129(a)) | |
| 1810 | 770 | 2810 | 385 | For each additional invention to be examined (37 CFR 1.129(b)) | |
| 1801 | 770 | 2801 | 385 | Request for Continued Examination (RCE) | |
| 1802 | 900 | 1802 | 900 | Request for expedited examination of a design application | |

Other fee (specify) _____

*Reduced by Basic Filing Fee Paid

SUBTOTAL (3) ($) 165.00

## SUBMITTED BY

(Complete *(if applicable)*)

| Name (Print/Type) | Ellsworth R. Roston | Registration No. (Attorney/Agent) | 16,310 | Telephone | 310-824-5555 |
|---|---|---|---|---|---|
| Signature | Ellsworth R. Roston | | | Date | 08/05/04 |

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CERTIFICATE OF MAILING UNDER 37 C.F.R. § 1.8

I hereby certify that this correspondence is being deposited with the United States Postal Service with sufficient postage as First Class Mail in an envelope addressed to: Mail Stop Appeal Brief - Patents, Commissioner for Patents, PO Box 1450, Alexandria VA 22313-1450 on August 5, 2004.

Donna M. Colon

Donna M. Colon

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

| | | |
|---|---|---|
| Appl. No. | : | 10/051,886 |
| Applicant | : | Valery V. Felmetsger |
| Filed | : | 04/06/2001 |
| Art Unit | : | 2827 |
| Examiner | : | Alonzo Chambliss |
| Title: | | PERMANENT ADHERENCE OF THE BACK END OF A WAFER TO AN ELECTRICAL COMPONENT OR SUB-ASSEMBLY |
| Docket No.: | : | SPUTT-57354 |
| Customer No. | : | 24201 |
| Confirmation No. | | 7950 |

Mail Stop Appeal Brief - Patents
Commissioner for Patents
P.O. Box 1450
Alexandria, VA 22313-1450

# APPEAL BRIEF

## I. Real Party in Interest

An executed assignment from Valery V. Felmetsger to Sputtered Films, Inc. was submitted to the USPTO with the application. This is evidenced by a postcard stamped by the USPTO on 01/16/02. However, applicant cannot find any evidence in the file that the assignment was recorded by the USPTO. Applicant will accordingly submit another copy of the assignment to the USPTO for recordation by the USPTO.

II. Related Appeals and Interferences

There are no related appeals or interferences.

III. Status of Claims

Claims 1 and 3-69 have been retained in the application. Claims 1 and 3-69 have been rejected under "35 U.S.C. 112, second paragraph" as being incomplete for omitting essential steps, such omission amounting to a gap between the steps. See MPEP 42172.01. The omitted steps are: "a wafer disposed on a wafer land and a lens shield that is spaced from to (sic) the wafer land since the lower powering step must include the combination of a wafer land and the lens shield in order to create argon ions forming microscopic roughness on the surface of the wafer." The Examiner's rejection of claims 1 and 3-69 under 35 U.S.C. 112, second paragraph has been discussed in Section VIII (E) of this Appeal Brief.

Claims 4, 6, 7, 14-16, 20, 21, 23, 34, 60-64 and 67 have been indicated as allowable over the prior art cited by the Examiner. The Examiner has objected to claims 4, 6, 7, 14-16, 20, 21, 23, 34, 60-64 and 67 as being dependent upon a rejected base claim but has indicated that these claims would be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims.

Claims 1-3 have been rejected under 35 U.S.C. 102(e) as being clearly anticipated by Akiyama patent 6,391,796.

Claim 5 has been rejected under 35 U.S.C. 102(a) as being clearly anticipated by the Admitted Prior Art.

Claims 9-12, 22, 23, 29, 31, 39, 41, 42, 44-58, 66, 68 and 69 have been rejected under 35 U.S.C. 103(a) as being unpatentable over Akiyama as applied to claim 5 and further in view of the Admitted Prior Art.

Claims 8, 13, 17-19, 24-28, 30, 31-33, 40, 42 and 43 have been rejected under 35 U.S.C. 103(a) as being unpatentable over Akiyama and the Admitted Prior Art as applied to claims 5, 11, 22, 29, 30 and 39 and further in view of Hong patent 6,375,810.

IV. Status of Amendments

A final rejection of the application was issued in an Office Action dated 04/20/04. Subsequent to the Office Action dated 04/20/04, applicant filed an amendment under Rule 116 on July 12, 2004 to make cosmetic changes in a few of the claims on the basis of errors noted by applicant's attorney in preparing an appeal brief in this application. Specifically, applicant made claim 6 dependent from claim 5. Applicant also amended claims 59 and 60 to make the recitations in the claims consistent with the disclosures in the specification.

The Examiner issued an Office Action on this amendment on 07/23/2004. In the Office Action, the Examiner indicated that (1) the proposed amendment would not be entered or (2) would be entered and an explanation would be provided of how the new or amended claims would be rejected as provided in the Office Action. The Examiner rejected the claims that he previously had rejected and objected to the claims that he had previously objected to. In view of this, applicant assumes that the Examiner has entered the proposed amendment.

Applicant also filed a supplemental amendment under Rule 116 on July 9, 2004 to make cosmetic changes in a few of the application claims on the basis of errors noted by applicant's attorney in preparing an appeal brief in this application. Specifically, applicant

amend claims 7 and 20 to make them consistent with the disclosure in the specification and consistent with the recitation in claims 4 and 7. Applicant also amended claim 50 to avoid any possibility of a duplicate recitation. On July 28, 2004, applicant filed a second supplemental amendment under Rule 116 to make minor amendments in a few of the claims. Applicant has not heard from the Examiner on either of these proposed amendments under Rule 116.

V. Summary of the Invention

The Examiner has rejected a number of the claims on the basis of "the Admitted Prior Art." In order for the Board of Appeals to assess properly the allegedly "Admitted Prior Art", applicant has included in this Section of the Appeal Brief the section of the application entitled "Background of the Preferred Embodiment of the Invention". The Summary of the Invention accordingly reads as follows:

## BACKGROUND OF THE PREFERRED EMBODIMENT OF THE INVENTION

Integrated circuit chips have been used widely in recent years to form electrical circuits which provide functions not previously capable of being attained. The integrated circuits have been formed by providing substrates on which a plurality of layers have been deposited to form a wafer. Electrical components or sub-assemblies have then been attached to the wafers to form integrated circuits. The electrical components are ordinarily not compatible with the wafers to which they are attached. The wafer surface has accordingly been cleaned and prepared to receive successive depositions of materials which will make the wafer surface compatible with the electrical components or sub-assemblies. For example, successive operations may be as follows:

1. A cleaning of the wafer surface as by etching;
2. A deposition of a layer of chromium on the wafer surface;
3. A deposition of a layer of nickel vanadium on the layer of chromium;
4. A deposition on the layer of nickel vanadium of a layer of a metal selected from the group consisting of copper, gold and silver; and
5. A soldering of the electrical component to the layer of the metal selected from the group consisting of copper, gold and silver.

The use of the successive layers as discussed above has been practiced for some time. However, there are problems in the use of these successive layers. A major problem has been that the electrical component or sub-assembly has not been permanently adhered to the wafer even with the use of all of the different layers specified above. The lack of permanent adherence results in part from the heat produced by the soldering of the metal layer to the electrical component and from thermal shock. Lack of permanent adherence may be seen by scratching the surfaces of the different layers specified above and/or by bending the layers. A

low adherence of the different layers leads to a lack of repeatability in the operating characteristics of the assembly including the wafer and the electrical component or assembly."

## BRIEF DESCRIPTION OF A PREFERRED EMBODIMENT OF THE INVENTION

This invention provides for a firm adherence of an electrical component or sub-assembly to a surface of a wafer by providing a firm adherence between layers intermediate the wafer and the electrical component or sub-assembly. Furthermore, the firm adherence is provided even when the layers deposited between the wafer surface and the electrical component or sub-assembly are subjected to tests to separate the layers. These tests include bending the layers and scratching the layers bent to determine the permanent adherence of the wafer and the electrical component or sub-assembly.

In a preferred embodiment of the invention, a plurality of successive layers are firmly adhered to one another and to a wafer surface and an electrical component or sub-assembly even when the wafer surface is not even and the layers are bent. The wafer surface is initially cleaned by an ion bombardment of an inert gas (e.g. argon) on the wafer surface in an RF discharge at a relatively high gas pressure. The wafer surface is then provided with a microscopic roughness by applying a low power and so that the inert gas (e.g. argon) ions do not have sufficient energy to etch the surface.

A layer of chromium is then sputter deposited on the wafer surface as by a DC magnetron with an intrinsic tensile stress and low gas entrapment by passing a minimal amount of the inert gas through the magnetron and by applying no RF bias to the wafer. The chromium layer is atomically bonded to the microscopically rough wafer surface. A layer of a nickel-vanadium alloy is deposited on the chromium layer and a layer of a metal selected from the group consisting of gold, silver and copper is deposited on the nickel-vanadium layer. The nickel-vanadium layer is deposited between the chromium layer and the metal layer with an intrinsic compressive stress by applying an RF bias to the wafer to neutralize the intrinsic tensile

stress of the chromium layer and any intrinsic stress of the metal layer. The electrical component is adhered as by solder to the metal selected from the group consisting of gold, silver and copper.

## BRIEF DESCRIPTION OF THE DRAWINGS

In the drawings:

Figure 1 is a schematic sectional view of a wafer having electrical circuits such as a transistor on a front surface and having layers of different materials deposited on a back surface to provide a compatible adherence between the back surface of the wafer and an electrical component or sub-assembly;

Figure 2 is an enlarged schematic sectional view showing the wafer disposed on a waferland and showing a bias voltage applied to the waferland and a lens shield disposed on the waferland;

Figure 3 is an enlarged schematic sectional view showing an adapter ring disposed between the wafer and the waferland when the waferland is oversized relative to the wafer;

Figure 4 is a schematic view in section of apparatus of the prior art for depositing layers of different materials on the back surface of the wafer to form the embodiment shown in Figure 1;

Figure 5 provides curves showing the relationship between the RF bias power applied to the wafer and the intrinsic stress imposed upon the wafer when a nickel vanadium layer constituting one of the layers shown in Figure 1 is deposited on the back surface of the wafer.

## DETAILED DESCRIPTION OF A PREFERRED EMBODIMENT OF THE INVENTION

In a preferred embodiment of the invention, a wafer generally indicated at 10 (Figure 1) may include a layer 12 illustratively formed from pure silicon, silicon dioxide and doped silicon with different crystal orientations. The wafer 10 may include a transistor 16 having electrical circuitry formed from a plurality of layers successively deposited on the front surface of the layer 12 in a conventional manner.

An electrical component or sub-assembly 14 is to be adhered to the back surface 17 of the layer 12. In this way, the transistor 16 and the electrical component or sub-assembly 14 can define electrical circuitry which performs specific functions. This electrical circuitry may be sufficient unto themselves to perform the specific functions or they may combine with other electrical circuitry to perform the specific functions. In Figure 1, the component or sub-assembly 14 is shown before it is permanently adhered to the wafer 10.

The layer 12 and the electrical component or sub-assembly 14 are ordinarily not compatible with each other in the sense that the component or sub-assembly cannot be adhered directly to the layer 12. Because of this, the electrical component or sub-assembly is to be permanently adhered mechanically to the wafer 10. This lack of permanent adherence may be particularly troublesome when it is desired to provide an electrical continuity with little or no impedance between the wafer 10 and the electrical component or sub-assembly 14. Because of this, the electrical component or sub-assembly is to be permanently adhered mechanically to the wafer 10.

In order to provide such a compatibility, a plurality of successive layers have been deposited in sequence in the prior art on the surface 17 of the layer 12. These successive layers

have included a layer 18 (Figure 1) of chromium, a layer 20 of nickel vanadium and a layer 22 of a metal selected from the group consisting of copper, gold and silver. The electrical component or sub-assembly 14 is then soldered to the metal layer 22.

Each of the layers 18, 20 and 22 has been allegedly compatible in the prior art with the adjacent layers. For example, the chromium layer 18 has been allegedly compatible in the prior art with the layer 22 and the nickel vanadium layer 20, and the layer 12 formed from a metal selected from the group consisting of copper, silver and gold has been allegedly compatible with the nickel vanadium layer 20 and the component or sub-assembly 14.

Even when the additional layers have been added between the layer 12 and the electrical component or sub-assembly 14 in the prior art, there has often not been good adherence between the wafer 10 and the component or sub-assembly. For example, the lack of adherence may be seen by scratching one or more of the different layers specified or by bending the different layers. The lack of adherence between the different layers becomes particularly pronounced when the electrical component or sub-assembly 14 is soldered to the layer 22 selected from the group consisting of copper, nickel and gold. This results from the large amount of heat developed during the soldering operation.

The preferred embodiment of this invention provides a wafer 10 including the layer 12 and an electrical component or sub-assembly 14 and layers of chromium, nickel vanadium and a metal selected from the group consisting of copper, gold and silver, the same layers as have been provided in the prior art. However, in the preferred embodiment of the invention, the layers have been formed to adhere the layer 12 firmly and permanently to the electrical component or sub-assembly 14.

In the preferred embodiment of the invention, the surface 17 of the layer 12 is cleaned in a unique manner and the layers of chromium, nickel vanadium and the metal selected from the group consisting of copper, gold and silver are sequentially deposited in a unique manner on the layer 12, so that the electrical component or sub-assembly is firmly and permanently adhered to the wafer. The layers 18, 20 and 22 are formed to provide this firm and permanent adherence to the layer 12.

As a first step in the preferred embodiment in applicant's method, a thin layer is removed from the back surface 17 of the layer 12 to eliminate any impurities in the surface. This removal is provided by an RF discharge in a combination of electrical and magnetic fields in a manner well known in the art and discussed subsequently in connection with Figure 4. The discharge is provided by a flow of molecules of an inert gas such as argon in the combined electrical and magnetic fields. The argon is ionized in the electrical and magnetic fields and the ions are attracted to the back surface 17 of the layer 12 to etch the layer surface. In the prior art, the argon molecules have been generally provided at a low gas pressure such as (1) $10^{-3}$ Torr and at a gas flow rate of approximately 15 standard cubic centimeters per minute (sccm). However, in applicant's preferred embodiment, the argon molecules are provided at a relatively high gas pressure such as approximately 4-6 $10^{-3}$ Torr and at a gas flow rate of approximately 40-50 sccm. This prevents the surface 10 from being atomically or microscopically smooth.

A high-power step is first provided to clean the surface 17 of the layer 12. In this high power step, approximately 600-1200 watts are applied between the waferland 24 (Figure 2) and a grounded lens shield 25 by an RF voltage from a source 21. Molecules of an inert gas such as argon are provided at a flow rate of approximately 40-50 sccm and at a temperature of approximately 320ÿ C. for a suitable period of time such as approximately 30 seconds. In this stage, impurities are removed from the wafer surface and an atomically rough surface is created on the wafer.

A subsequent step in the etching process provides for the creation of a microscopic or atomic roughness on the back surface 17 of the layer 12. This is provided in a relatively low power step involving the application of approximately 50-100 watts between the waferland 24 and an electrically grounded lens shield 25 in Figure 2. In Figure 2, the lens shield 25 is spaced from the waferland 24. Because of the relatively low power, the argon ions do not have sufficient energy to remove much material from the surface 17 of the layer 12. Instead, the argon ions have sufficient energy to create a microscopic or atomic roughness on the surface. The creation of the microscopic or atomic roughness on the surface 17 of the layer 12 may be obtained by providing a flow of argon at approximately 40-50 sccm for a period of approximately 60 seconds. The creation of the microscopic or atomic roughness on the wafer surface 10 constitutes an important feature of applicant's preferred method of the invention. The step discussed in this paragraph causes the roughness of the surface to be increased relative to the roughness produced in the wafer surface by the step in the previous paragraph.

As shown in Figure 2, the wafer 10 is disposed on a waferland 24 and a lens shield 25 is disposed in abutting relationship to the waferland 24 and is grounded. The waferland 24 and the lens shield 25 are covered with a chromium layer to prevent atoms of the material of the waferland and the lens shield from contaminating the chromium layer which is subsequently applied to the wafer 10. The covering of the waferland 24 and the lens shield 25 with the chromium layer is believed to constitute one of the novel features of the preferred embodiment of this invention.

When the waferland 24 is relatively large in comparison to the size of the wafer 10, an adapter ring 26 (Figure 3) may be disposed on the waferland to adapt the size of the wafer to the size of the waferland. The adapter ring is also coated with a layer of chromium before the deposition of the chromium layer on the wafer 10 to prevent molecules of material from the adapter ring from contaminating the layers subsequently deposited on the chromium layer 18.

A layer 18 of chromium having a thickness such as approximately four hundred Angstrom (400Å ) is next deposited on the surface 17 of the layer 12. A good adhesion is provided between the chromium layer 18 and the back surface 17 of the layer 12 because of the microscopic or atomic roughness of the surface 17. This results from the fact that the microscopic roughness creates a good atomic or electrical bond with the chromium layer 18. The chromium layer 18 is deposited on the surface 17 of the layer 12 with a relatively low intrinsic stress. This stress may be tensile. The chromium layer 18 provides an adhesion to the surface 17 and to the nickel vanadium layer 20 which is subsequently deposited on the chromium layer.

The chromium layer 18 is deposited at a low rate of flow of an inert gas such as argon. This low rate may be in the order of 3-5 sccm. This prevents argon atoms from being entrapped in the layer 18. The presence of argon in the chromium layer 18 is not desirable because, during the soldering process, the argon molecules tend to destroy the adhesion of the chromium layer with the back surface 17 of the layer 12 and the nickel vanadium layer 20 subsequently deposited on the chromium layer. Power in the order of 4000 watts may be applied to the sputtering targets in the magnetron during the chromium deposition. The time for the formation of the chromium layer 18 may be in the order of 7 seconds.

The nickel vanadium layer 20 is deposited on the chromium layer 18, preferably in a thickness in the order of four thousand Angstrom (4000Å). The nickel vanadium layer is deposited on the chromium layer with a low intrinsic stress. This intrinsic stress is compressive to counteract or balance the intrinsic tensile stress provided by the chromium layer 18. The nickel vanadium layer 20 is provided with a low intrinsic stress because the nickel vanadium is deposited on the chromium layer 18 with an RF bias power of approximately 300 watts between the waferland 24 and the lens land 25.

Figure 5 is a curve 32 showing the relationship between RF bias power in watts along the horizontal axis and stress in E9 dynes per square centimeter along the vertical axis when the nickel vanadium layer 20 is deposited on the chromium layer 18. The curve 32 shown in Figure 5 is provided for deposition equipment such as the equipment shown in Figure 4. Figure 5 shows how the stress in the nickel - vanadium layer 20 decreases with increases in the RF power applied.

The curve 36 in Figure 5 is provided for a thickness of approximately 4000 Angstrom in the nickel vanadium layer 20. A zero stress is produced in the nickel vanadium layer 20 at an RF bias power of approximately 250 watts when the thickness of the nickel vanadium layer 20 is approximately 4000 Angstrom. As an example, a deposition of the nickel vanadium layer 20 may be provided with a power of approximately 6000 watts, with a flow rate of argon at approximately 5 sccm, with RF power of approximately 300 watts, with an anode voltage of approximately 60 volts and with a duration time of approximately 50 seconds.

The layer 22 of the metal selected from the group consisting of copper, gold and silver is thereafter deposited on the nickel vanadium layer 20. The layer 22 may be deposited in a conventional manner well known in the art. Preferably the thickness of the layer 22 is approximately five hundred Angstroms (500Å). The layer 22 formed from the metal selected from the group consisting of copper, gold and silver is deposited on the nickel vanadium layer 20 with as low an intrinsic stress as possible. It is difficult to control the stress in the metallic layer 22 directly. Instead, the stress in the layer 22 is controlled by regulating the stress in the nickel vanadium layer 20. As will be appreciated, this can be accomplished by providing the layer 20 with the proper thickness. The method of depositing the layer 22 on the layer 20 can be the same as that performed in the prior art. For example, the power applied to obtain the deposition of a copper layer may be approximately 4000 watts; the argon may be provided at a flow rate of approximately 9 sccm; and the time for the deposition may be approximately 8 seconds.

To adhere the layer 22 to the component or sub-assembly 14, hot liquid solder is disposed on the surface of the component or sub-assembly. The solder may be an amalgam of tin and lead. While the solder is hot and liquid, the layer 22 is adhered to the component or sub-assembly 14 and is maintained in firm position on the component or sub-assembly until the solder solidifies and cools.

Tests have been conducted on depositions formed by the preferred methods of this invention and the depositions formed by the methods of the prior art. One test has involved the scratching of the depositions and the subsequent testing of the depositions for peeling. No peeling occurred in the depositions formed by the preferred method of this invention. From half peeling to complete peeling occurred in the depositions formed by the method of the prior art. Another test has involved the bending of the depositions. This test has been particularly provided to determine the adherence of the nickel vanadium layer relative to the adjacent layers of chromium and the metal selected from the group consisting of copper, gold and silver. The adhesion in the layer of the deposition formed by the methods of this invention continued at 100% even after the bending. However, the adherence decreased to approximately 36%-59% in the depositions produced by the methods of the prior art.

The layers 18, 20 and 22 may be deposited on the wafer surface 12 by conventional equipment. For example, this equipment is disclosed in patent 5,766,426 issued on June 16, 1998, and assigned of record to the assignee of record of this application. This equipment is schematically illustrated in Figure 4 and is generally indicated at 48 in Figure 4. This equipment may include the waferland 24 for receiving the wafer. If the waferland 24 is outsized relative to the wafer, the wafer 10 may be disposed on the adaptor ring 26 (Figure 3) and the adaptor ring may be disposed on the waferland. An RF voltage may be applied to the waferland 24 from one terminal of the RF supply 21, the other terminal of which is grounded as at 27. A shield 50 may be disposed in contiguous relationship to the waferland 24 and may be

grounded. The shield may be grounded as at 27 to limit any stray movements of charged particles.

Targets 52 and 54 may be spaced from the shield 50 and may be provided with a suitable configuration such as a hollow frusto-conical configuration. The target 52 may be more closely spaced to the shield 50 than the target 54 and may be disposed on the same axis as the target 54. The target 52 may be provided with a greater radius than the target 54. The targets 52 and 54 may be made from the material which is to be deposited in a layer on the surface 12 of the layer. For example, the targets 52 and 54 may be made from chromium when the chromium layer 18 is to be deposited on the surface 17 of the layer 12.

An anode 56 is disposed in a spaced relationship from the target 54, preferably in a coaxial relationship with the targets 52 and 54. A cavity 57 is produced between the anode 56 and the targets 52 and 54. A positive voltage may be produced between the anode 56 and the targets 52 and 54 as from a voltage source 58. This voltage difference between the anode and the targets 52 and 54 produces an electrical field. The electrical field causes electrons to be produced in the cavity 57 defined by the anode 56 and the targets 52 and 54. Magnets 60 and 62 may be respectively disposed relative to the targets 52 and 54 to produce magnetic fields in a substantially perpendicular relationship to the electrical field between the anode 56 and the targets 52 and 54.

VI. Issues

The issues with respect to the claims under rejection are as follows:

1. Does applicant have to recite in each of claims 1 and 3-59 language similar to the following as proposed by the Examiner in Section 4 on page 4 of the Office Action dated 04/20/04 --

"a wafer disposed on a wafer land and a lens shield that is spaced from to (sic) the wafer land"?

2. Is the following language recited in a number of applicant's claims sufficient to overcome the rejection by the Examiner of claims 1 and 3-69 under 35 U.S.C. 112, second paragraph, which claims recite a microscopic roughness produced on the surface of the wafer by providing ions of an inert gas with an insufficient energy to etch the surface of the wafer but with a sufficient energy to create the microscopic roughness on the surface of the wafer?

3. Even if the Examiner is correct that applicant's claims have to recite a "wafer disposed on a wafer land and a lens shield that is spaced from to (sic) the wafer land", does this requirement apply to all of applicant's claims including (a) claims that do not recite a microscopic roughness on the surface of the wafer and (b) claims that recite a microscopic roughness on the surface of the wafer without specifying how the microscopic roughness is produced?

4. Is a method step patentable of creating a microscopic roughness on a surface of a wafer to receive a deposition of the material on the surface of the wafer by providing ions of an inert gas with an insufficient energy to etch the surface of the wafer but with a sufficient energy to create the microscopic roughness on the surface of the wafer?

5. Is a method step patentable of depositing a chromium layer with a low intrinsic tensile stress on a cleaned surface of a wafer?

6. Is a method step patentable of depositing a chromium layer with a low intrinsic tensile strength on a wafer surface having a microscopic roughness?

7. Is a method patentable of (a) creating a microscopic roughness on a surface of a wafer to receive a deposition of a material on the wafer surface by providing ions of an inert gas with an insufficient energy to etch the surface of the wafer but with insufficient energy to create the microscopic roughness on the surface of the layer and (b) then depositing a layer of chromium with a low intrinsic stress on the microscopically rough surface of the wafer?

8. Is the method set forth in paragraph 7 patentable where the chromium layer is deposited on the surface of the wafer in a magnetron and with a low flow rate of molecules of an inert gas in the magnetron?

9. Is a method as set forth in paragraph 6 patentable wherein a chamber is provided in which to perform the recited steps and wherein molecules of an inert gas flow through the chamber in an order of three (3) to five (5) standard cubic centimeters per minute (3-5 sccm)?

10. Is a method as set forth in paragraph 8 patentable where a chamber is provided in which to perform the recited steps and wherein molecules of an inert gas flow through the chamber in an order of three to five standard cubic centimeters per minute (3-5 sccm)?

11. Is a method patentable of depositing a chromium layer with a low intrinsic tensile stress on a clean surface of a wafer and then depositing a layer of nickel vanadium on the surface of the wafer with a low intrinsic compression stress to neutralize the low intrinsic stress of the chromium layer?

12. Is a method as set forth in paragraph 6 patentable where a layer of nickel vanadium is deposited on the surface of the chromium layer with a low intrinsic compressive stress to neutralize the low intrinsic tensile stress of the chromium layer?

13. Is a method as set forth in paragraph 7 patentable where a layer of nickel vanadium is deposited on the surface of the chromium layer with a low intrinsic compressive stress to neutralize the low intrinsic tensile stress of the chromium layer?

14. Is a method as set forth in paragraph 8 patentable where a layer of nickel vanadium is deposited on the surface of the chromium layer with a low intrinsic compressive stress to neutralize the low intrinsic tensile stress of the chromium layer?

15. Is a method as set forth in paragraph 9 patentable where a layer of nickel vanadium is deposited on the surface of the chromium layer with a low intrinsic compressive stress to neutralize the low intrinsic tensile stress of the chromium layer?

16. Is a method as set forth in paragraph 10 patentable where a layer of nickel vanadium is deposited on the surface of the chromium layer with a low intrinsic compressive stress to neutralize the low intrinsic tensile stress of the chromium layer?

17. Is a method as set forth in paragraph 11 patentable where an RF bias power is applied during the deposition of the nickel vanadium layer on the chromium layer with a low intrinsic compressive stress to neutralize the low intrinsic tensile stress of the chromium layer?

18. Is a method as set forth in paragraph 12 patentable where an RF bias power is applied during the deposition of the nickel vanadium layer on the chromium layer with a low intrinsic compressive stress to neutralize the intrinsic tensile stress of the chromium layer?

19. Is a method as set forth in paragraph 13 patentable where an RF bias power is applied during the deposition of the nickel vanadium layer on the chromium layer with a low intrinsic compressive stress to neutralize the low intrinsic tensile stress of the chromium layer?

20. Is a method as set forth in paragraph 14 patentable where an RF bias power is applied during the deposition of the nickel vanadium layer with a low intrinsic compressive stress to neutralize the low intrinsic tensile stress of the chromium layer?

21. Is a method as set forth in paragraph 15 patentable where an RF has power is applied during the deposition of the nickel vanadium layer on the chromium layer with a low intrinsic compressive stress to neutralize the low intrinsic tensile stress of the chromium layer?

22. Is a method as set forth in paragraph 16 patentable where an RF bias power is applied during the deposition of the nickel vanadium layer on the chromium layer with a low intrinsic compressive stress to neutralize the intrinsic tensile stress of the chromium layer?

VII. Grouping of Claims

A. Grouping of Claims as Proposed by the Examiner

In the Office Action dated 04/20/04, the Examiner grouped the claims as follows:

1. Group 1

Claims 1-3 rejected under 35 U.S.C. 102(e) as being clearly anticipated by Akiyama patent 6,391,796. However, applicant cancelled claim 2 in an amendment filed on January 23, 2003.

2. Group 2

Claim 5 rejected under 35 U.S.C. 102(e) as being clearly anticipated by the allegedly Admitted Prior Art.

3. Group 3

Claims 9-12, 22, 23, 29, 31, 39, 41, 42, 44-58, 66, 68 and 69 have been rejected under 35 U.S.C. 103(a) as being unpatentable over Akiyama patent 6,391,796 as applied to claim 5 and further in view of the allegedly Admitted Prior Art.

4. Group 4

Claims 8, 13, 17-19, 24-28, 30, 31-33, 40, 42 and 43 have been rejected under 35 U.S.C. 103(a) as being unpatentable over Akiyama patent 6,391,796 and the allegedly Admitted Prior Art as applied to claims 5, 11, 22, 29, 30 and 39 and further in view of Hong patent 6,375,819.

5. Group 5

Claims 1 and 3-69 have been rejected under 35 U.S.C. 112, second paragraph, as being incomplete for omitting "essential steps" consisting of "a wafer disposed on a wafer land and a lens shield that is spaced from to (sic) the wafer land. The Examiner has predicated this rejection on the ground that "the lower powering step must include the combination of a wafer land and the lens shield in order to create argon atoms forming microscopic roughness on the surface of the wafer."

B. Grouping of Claims as Proposed by Applicant

Claims 9-12, 22, 23, 29, 31, 39, 41, 42, 44-58, 66, 68 and 69 do not stand or fall together as the Examiner has specified in the Office Action dated 04/02/04. This may be seen from the following analysis:

Subgroup a: Claims 9, 10, 48, 49, 50, 53, 54, 56, 57, 58

Layer of chromium deposited on a wafer surface with a low intrinsic tensile stress.

Layer of nickel vanadium deposited on the chromium layer with a low intrinsic compressive stress.

No recitation of microscopic roughness of wafer surface

Subgroup b: Claims 22, 23

Microscopic roughness on wafer surface

Layer of chromium deposited on wafer surface with a low intrinsic tensile stress

Layer of nickel vanadium deposited on the chromium layer with a low intrinsic compressive stress

Subgroup c: Claims 12, 29, 31, 33, 41, 44, 45, 47, 51, 52, 55

Microscopic roughness on wafer surface

Layer of chromium deposited on the microscopically rough surface of the wafer with a low intrinsic tensile stress

No layer of nickel vanadium recited

Subgroup d: Claims 42, 66, 69

Microscopic roughness on surface of wafer

Microscopic roughness is provided on the surface of wafer by disposing the wafer in a chamber and by passing ions of an inert gas through the chamber with insufficient energy to etch the surface of the wafer but with sufficient energy to produce the microscopic roughness on the surface of the wafer.

Layer of chromium deposited on the microscopically rough wafer surface with a low intrinsic tensile stress.

No layer of nickel vanadium recited.

Subgroup e: Claim 11

No microscopic roughness on surface of wafer,

Chromium layer deposited on surface of wafer with a low intrinsic tensile stress.

No layer of nickel vanadium on chromium layer

Subgroup f: Claim 68

Microscopic roughness on surface of wafer

Microscopic roughness provided on surface of wafer by providing ions of an inert gas with insufficient energy to etch the surface of the wafer but with sufficient energy to produce the microscopic roughness on the surface of the wafer.

Layer of chromium deposited on microscopically rough surface of wafer with a low intrinsic tensile stress.

Layer of nickel vanadium deposited on surface of chromium layer with a low intrinsic compressive stress.

As will be seen from the above analysis, the claims in group (VII)(A)(3) as proposed by the Examiner can be divided into six (6) subgroups a-f. Claims 8, 13, 17-19, 24-28, 30, 31-33, 40, 42 and 43 in group (VII)(A)(4) as proposed by the Examiner do not stand or fall together for the same reasons as discussed above with respect to the claims in group (VII)(A)(3). The claims in groups (VII)(A)(3) and (VII)(A)(4) can be divided into subgroups (a)-(f) as follows:

Group a: Claims 8, 9, 10, 17, 18, 19, 24, 48, 49, 53, 54, 56, 57 and 58

(i) a wafer surface in which no microscopic roughness is recited, (ii) a chromium layer with a low intrinsic tensile stress is deposited on the wafer surface and (iii) a nickel vanadium layer is deposited with a low intrinsic compressive stress on the chromium layer. Claim 48 is representative of the claims in this subgroup.

Subgroup b: Claims 22, 23, 25, 26, 27, 28, 50

(i) a wafer surface having a microscopic roughness, (ii) a layer of chromium deposited on the surface of the microscopic roughness with a low intrinsic tensile stress and (iii) a layer of nickel vanadium deposited on the chromium layer with a low intrinsic compressive stress. Claim 22 is representative of the claims in this subgroup.

Subgroup c: Claims 12, 29, 30, 31, 41, 44, 45, 47, 51, 52, 55

(i) a wafer surface having a microscopic roughness, (ii) a layer of chromium deposited on the wafer surface of microscopic roughness and (iii) no recitation of a nickel vanadium layer. Claim 29 is representative of the claims in this subgroup.

Subgroup d: Claims 32, 42, 43, 46, 66, 69

Claims 42, 43, 46 and 69 are dependent from claim 39 in sub group c. Claims 32 and 66 are respectively dependent from claims 30 and 29. All of these claims further recite that the microscopic roughness is provided on the surface of the wafer by providing ions of an inert gas with an insufficient energy to etch the surface of the wafer but with a sufficient energy to produce the microscopic roughness on the surface of the wafer. They additionally recite a layer of chromium deposited on the microscopically rough surface of the wafer with a low intrinsic tensile stress. They do not recite a layer of nickel vanadium deposited on the chromium layer. Claim 43 is representative of the claims in this subgroup.

Subgroup e: Claim 68

Claims (i) a wafer surface having a microscopic roughness by providing ions or an inert gas with an insufficient energy to etch the wafer surface but with a sufficient energy to produce the microscopic roughness on the wafer surface, (ii) a layer of chromium deposited on the microscopically rough surface of the wafer with a low intrinsic tensile stress and (iii) a layer of nickel vanadium

deposited on the surface of the chromium layer with a low intrinsic compressive stress.

Subgroup f: Claims 11, 13

Claims a clean surface of a wafer and a layer of chromium deposited on the clean surface of the wafer with a low intrinsic tensile stress. Does not claim a microscopically rough surface on the wafer and does not claim a nickel vanadium layer deposited on the chromium layer. Claim 13 is representative of the claims in this group.

The claims in each of the subgroups a, b, c, d, e and f are patentably distinct from the claims in the other subgroups. Because of this, if all of the claims in the subgroups a, b, c, d e and f are compiled in a single group as the Examiner has done, a holding of non-patentability with respect to any one of the claims in any one of the subgroups would cause the claims in the other subgroups to be held non-patentable even though the claims in each subgroup are patentably distinct from the claims in the other subgroups.

VIII. Argument

A. Akiyama patent 6,391,796

Applicant's method includes a step of removing a thin layer from a surface of a wafer to eliminate any impurities from the surface of the wafer and thereafter creating a microscopic roughness on the surface of the wafer by providing ions of an inert gas with an insufficient energy to etch the surface of the wafer but with a sufficient energy to create the microscopic roughness on the surface of the wafer. The chromium layer is then deposited on the microscopically rough surface of the wafer. Applicant recites the creation of the microscopic

roughness on the surface of the wafer in such claims as claims 1, 3, 4, 32, 35-38, 42, 43, 46, 66, 68 and 69.

Akiyama heat treats a silicon wafer under a reducing atmosphere using a rapid heating rapid cooling apparatus after a natural oxide film on the silicon wafer surface has been removed. In the rapid heating, rapid cooling apparatus, the silicon wafer is subjected to a heat treatment under an atmosphere of 100% hydrogen or a mixed gas atmosphere of argon and/or nitrogen containing 10% or more of hydrogen. (Akiyama col. 2, lines 20-42.) This method is not the method that applicant uses to produce the microscopic roughness of the wafer surface.

In the last sentence of the third (3d) paragraph on page 2 of the Office Action dated 04/20/04, the Examiner states the following:

> "Furthermore, nowhere in the MPEP does it state that a reference has to state word for word the claimed limitation."

Thus, after previously stating in the same paragraph that Akiyama discloses what applicant has set forth in the specification and recited in the claims, the Examiner appears to concede on second thought that Akiyama does not disclose what applicant has disclosed and has recited in the claims.

Applicant recites in a number of the rejected claims the method that the Examiner is requiring on page 4 of the Office Action dated 04/20/04 by the language "a wafer land and a line shield from to (sic) the wafer land." The method recited by applicant is that applicant creates a microscopic roughness on the wafer surface by providing ions of an inert gas with an insufficient energy to etch the wafer surface but with a sufficient energy to create the microscopic roughness on the wafer surface. Applicant prefers his approach to that of the Examiner because applicant's

approach is broader than the Examiner's approach and more truly represents how the method obtains the desired results.

B. The Admitted Prior Art

The Formation of a Chromium layer with a Low Tensile Stress

In paragraph 7 of the Office Action dated 04/20/04, the Examiner has defined the Admitted Prior Art in applicant's specification as pages 1 and 2 in their entirety, page 7, lines 5-14 and page 8, lines 6-10. Applicant disagrees that page 8, lines 8-10 constitutes Admitted Prior Art since it specifically discusses the preferred embodiment of the invention. Furthermore, the discussion on page 8 occurs after the heading "DETAILED DESCRIPTION OF A PREFERRED EMBODIMENT OF THE INVENTION" at the top of page 6 of the specification.

Applicant has indicated the following in the so-called Admitted Prior Art:

> "3. A deposition of a layer of chromium on the wafer surface;" (page 2, line 4).
>
> For example, the chromium layer 28 has been allegedly compatible in the prior art with the layer 22 and the nickel vanadium layer 20...(Page 7, lines 11 and 12)." (Underlining supplied.)

These are the only references in the so-called Admitted Prior Art to the chromium layer.

In the so-called Admitted Prior Art, applicant specifically discloses that the layers are not permanently bonded to one another. This may be seen from the discussion on page 6, lines 8-13 to page 8, line 5. This is why applicant has used the word "allegedly" in the quotation above from page 7, lines 11 and 12 of applicant's specification and why applicant has underlined the word "allegedly" in the quotation. The word "allegedly" has also been used in lines 10 and 11 on page 7 of applicant's specification:

"Each of the layers 18, 20 and 22 has been allegedly compatible in the prior art with the adjacent layers."

In the remainder of the next paragraph on page 7 (lines 10-14), applicant reiterates that the different layers are not permanently adhered to one another in the prior art. This may be seen from the use of the word 'allegedly" on page 7, line 11 and on page 11, line 13.

In the paragraph (page 8, lines 6-11), applicant emphasizes one of the features constituting applicant's invention. The emphasis occurs in the following sentence on page 8, lines 9-11:

"However, in the preferred embodiment of the invention, the layers have been formed to adhere the layer 12 firmly and permanently to the electrical component or sub-assembly 14." (Underlining supplied).

The last sentence in the next paragraph (page 8, lines 12-17) of applicant's specification re-affirms what applicant considers to constitute his invention. This sentence reads as follows:

"The layers 18, 20 and 22 are formed to provide this firm and permanent adherence to the layer 12." (Underlining supplied).

Applicant's layer 18 of chromium has a number of patentable distinctions over the prior art. Individual ones of these patentable distinctions are disclosed in applicant's specification and recited in applicant's claims. These distinctions include the following:

1. The layer 18 is adhered to the surface 17 of microscopic roughness on the layer 12 to provide an atomic or electrical bond with the surface 17.

2. The layer 18 of chromium is deposited on the surface 17 with a low tensile stress.

3. The chromium layer 18 is deposited at a low flow rate of an inert gas such as argon. This low flow rate may be in the order of 3-5 sccm. This prevents argon atoms from being entrapped in the chromium layer 18.

According to the Examiner on page 3 of the Office Action dated 04/20/04:

"The chromium layer has a low intrinsic tensile stress since the composition of the material has a tensile load. Also, since applicant has not recited in the claim how the chromium layer is neutralize (sic) the examiner views neutralizing as covering the chromium layer."

The language quoted above is incomprehensible. At any rate, as applicant has previously indicated, there is no disclosure in the Admitted Prior Art that the chromium layer has an intrinsic tensile stress. Furthermore, contrary to the position of the Examiner in the above quotation, the intrinsic tensile stress of the chromium layer in applicant's invention is neutralized by the compressive stress of the nickel vanadium layer and thus is recited by applicant in a number of the claims. Furthermore, the Examiner has not cited any prior art reference which states the following:

"The chromium layer has a low intrinsic tensile stress since the composition of the material has a tensile load."

If this is well known, the Examine should be able to cite without any difficulty a prior art reference which supports the Examiner's statement. Until the Examiner cites such a prior art reference, the Examiner's statement as quoted above should not be given any great credence.

Applicant respectfully submits that the Examiner should be required to cite prior art which supports his statement that "the composition of the material has a tensile load." Furthermore, the Examiner should be required to clarify what he has meant by this statement.

C. The Formation of a Nickel Vanadium layer with a Low Compressive Stress

Applicant states the following on page 2, line 5 of the Admitted Prior Art:

"3. A deposition of a layer of nickel vanadium on the layer of chromium."

Applicant then states in the Admitted Prior Art on page 2, lines 10-18 that the different layers in the Admitted Prior Art are not permanently adhered to one another. On page 8, lines 9-11 applicant states a synopsis of his invention.

"However, in the preferred embodiment of the invention, the layers have been formed to adhere the layer 12 firmly and permanently to the electrical component or sub-assembly 14." (Underlining supplied.)

The following are the features which patentably define the nickel vanadium layer over the prior art.

1. "The nickel vanadium layer is deposited on the chromium layer with a low intrinsic stress. This intrinsic stress is compressive to counteract or balance the intrinsic tensile stress provided by the chromium layer 18." (See page 12, lines 8-10 of applicant's specification). (Underlining supplied).

2. "The nickel vanadium layer is provided with a low intrinsic compressive stress because the nickel vanadium is deposited on the chromium layer 18 with an RF bias power of approximately 300 watts between the waferland 24 and the lens land 25." (See page 12, lines 11-13).

As applicant indicates on page 13, lines 1-2:

Figure 5 shows how the stress in the nickel-vanadium layer 20 decreases with increases in the RF power applied."

This is not disclosed in the prior art including the Admitted Prior Art.

D. The Failure of Hong to Disclose What the Examiner States that Hong discloses

On page 9 of the Office Action dated 04/20/04, the Examiner states:

"However, Hong discloses a metal layer deposited on the surface of the wafer in a magnetron with no RF or with a RF in the magnetron and with a low flow rate (i.e. rate sufficient to deposit the metal layer) of molecules of an inert gas (i.e. argon) in the magnetron (see col. 1 lines 22-55 and col. 2 lines 1-39). Thus, any metal layer (i.e., chromium) can be deposited by the process of Hong, since any type of metal layer can not be ionized utilizing an environment with no RF bias or with a RF bias in the magnetron yielding a uniform deposition of metal."

First of all, the quotation above is incomprehensible. Applicant would appreciate it if the Examiner would clarify what he intended to state in the above quotation. Secondarily, col. 1, lines 22-55 and col. 2, lines 1-39 in Hong constitute background to the Hong invention. This background is so basic that it constitutes the equivalent of what would be taught in a beginner's class in the field of deposition techniques. Contrary to the position of the Examiner, Hong does not teach anything in columns 1 and 2 which would cause Hong to be applicable to any of the novel features of any one of claims 8, 13, 17, 24-27, 30-31, 33, 40, 42, and 65 against which Hong has been cited as prior art.

E. The Rejection of Claims 1 and 3-69 Because of the Alleged Failure of Applicant to Recite an Essential Step in the Claims

The Examiner has "rejected claims 1 and 3-69 under 35 U.S.C. 112, second paragraph as being incomplete for omitting essential steps, such omission amounting to a gap between the steps. See MPEP §2712.01. The omitted steps are, "a wafer disposed on a wafer land and a lens shield that is spaced from to (sic) the wafer land" since the lower powering step must include the combination of a wafer land and the lens shield in order to create argon ions forming microscopic roughness on the surface of the wafer."

Applicant is not required to specify the use of the wafer land and the lens shield to produce a wafer surface with a microscopic roughness. Instead, applicant has recited a proper method step involving the creation of a microscopic roughness on the surface of the wafer by providing ions of an inert gas with an insufficient energy to etch the surface of the wafer but with a sufficient energy to create the microscopic roughness on the surface of the wafer. Applicant respectfully submits that this recitation meets the requirements of MPEP §2172.01.

MPEP §2172.01 states the following:

> "A claim which omits matter disclosed to be essential to the invention as described in the specification or in any other statements of record may be rejected under 35 U.S.C. 112, first paragraph, as not enabling." (Underling supplied).

Applicant does not disclose in the specification that the use of the wafer land and the lens shield to create the microscopic roughness on the surface of the wafer is "essential". Therefore, MPEP §2172.01 is not applicable. This is particularly true since applicant recites in the claims that applicant provides the microscopic roughness on the surface of the wafer by providing ions of an inert gas on the surface of the wafer with an insufficient energy to etch the surface of the wafer

but with a sufficient energy to produce the microscopic roughness on the surface of the wafer. Applicant respectfully submits that this is a true method step and that it recites how applicant produces the microscopic roughness on the surface of the wafer.

The alleged method proposed by the Examiner is not actually a method step. The alleged method proposed by the Examiner recites apparatus limitations and, is proper for inclusion in apparatus claims. Only claims 44-58 in this application constitute apparatus claims.

Even if the Examiner's position under 35 U.S.C. § 112, second paragraph, should be sustained by the Board of Appeals, this would affect only a relatively few of the claims. This may be seen from the following:

1. Claims 4, 6, 7, 14-16, 20, 21, 23, 34, 60-64 and 67 have been allowed by the Examiner if rewritten in independent form including all of the limitations of the base claim and any intervening claims.
2. A number of the claims recite a wafer surface but do not recite that the wafer surface has a microscopic roughness. These include claims 5, 8, 11, 13, 17-18, 19, 48, 49, 50, 53, 54, 56, 57, 58 and 59. It is recognized that an applicant does not have to recite every limitation in every claim. Therefore, it is proper for applicant to recite the wafer surface without reciting that the wafer surface has a microscopic roughness. The claims are accordingly not affected by the requirement of the Examiner to recite the alleged step of "a wafer disposed on a wafer and a lens shield that is spaced from to (sic) the wafer land."
3. A number of the claims recite that the wafer surface has a microscopic roughness but do not recite how the microscopic roughness is formed.

These include claims 6, 9, 10, 12, 22, 24, 25, 26, 27, 28, 29, 30, 31, 33, 39, 40, 41, 44, 45, 47, 51, 52, 55 and 65. It is proper for applicant to recite that the wafer surface has a microscopic roughness without reciting how the microscopic roughness is produced. These claims are accordingly not affected by the requirement of the Examiner to recite the alleged step of a "wafer disposed on a wafer land and a lens shield that is spaced from to (sic) the wafer land."

F. The Distinctions of the Claims Over the Prior Art

As will be seen from the above, there are a number of distinctions between the recitations in applicant's claims and the prior art cited by the Examiner. These distinctions are summarized below. Each of the distinctions listed below is not disclosed in any of the references (including the Admitted Prior Art) cited by the Examiner to reject the claims, whether the references are used individually or in combination. The distinctions include the following:

1. Creating a microscopic roughness on a surface of a wafer to receive a deposition of chromium on the wafer surface by providing ions of an inert gas with an insufficient energy to etch the surface of the wafer but with a sufficient energy to create the microscopic roughness on the surface of the wafer. Then depositing a layer of chromium with a low intrinsic stress on the microscopically rough surface of the layer.

2. Depositing a layer of chromium with a low intrinsic tensile stress on a surface of a wafer. The surface of the wafer is not recited as being microscopically rough.

3. Depositing a layer of chromium on a microscopically rough surface of the wafer. The method of producing the microscopic roughness is not recited in the claim.

4. Providing a flow of an inert gas at a low rate on the wafer surface when the chromium layer is deposited on the surface of the wafer, thereby to minimize the presence of the inert gas in the chromium layer.

5. Depositing the chromium layer on the surface of the wafer in a magnetron with no RF bias in the magnetron and with a low flow rate of molecules of an inert gas in the magnetron.

6. Providing a chamber in which to perform the recited steps and passing molecules of an inert gas flow through the chamber in the order of three (3) to five (5) standard cubic centimeters per minute (3-5 sccm).

7. Depositing a layer of nickel vanadium on the chromium layer with a low intrinsic compressive stress.

8. Depositing a layer of nickel vanadium on the chromium layer with a low intrinsic compressive stress to neutralize the low intrinsic tensile stress of the chromium layer.

9. Depositing a nickel vanadium layer on the surface of the chromium layer with an RF bias power to produce a low intrinsic compressive stress in the nickel vanadium layer for neutralizing the low intrinsic tensile stress in the chromium layer.

Claims 1, 3, 5, 8-13, 17-19, 22, 24-33, 35-59, 65 and 66 have been rejected in view of the prior art cited by the Examiner. Each of these claims is allowable over the cited prior art because of particular distinctions specified above as paragraphs VII(F)(1-9). The distinctions causing each of the claims to be allowable over the cited references are specified below:

Claim 1

(VIII)(F)(1)

Claim 3

(VIII)(F)(1)

Claim 5

(VIII)(F)(2), (VIII)(F)(7)

Claim 8

(VIII)(F)(2), (VIII)(F)(3)

Claim 9

(VIII)(F)(3), (VIII)(F)(7), (VIII)(F)(8)

Claim 10

(VIII)(F)(3), (VIII)(F)(7), (VIII(F)(8)

Claim 11

(VIII)(F)(2)

Claim 12

(VIII)(F)(2), (VIII)(F)(3)

Claim 13

(VIII)(F)(2), (VIII)(F)(5)

Claim 17

(VIII)(F)(2), (VIII)(F)(7), (VII)(F)(8)

Claim 18

(VIII)(F)(2), (VIII)(F)(7), (VIII)(F)(8)

Claim 19

(VIII)(F)(2), (VIII)(F)(7), (VIII)(F)(8)

Claim 22

(VIII)(F)(3), (VIII)(F)(7)

Claim 24

(VIII)(F)(3), (VIII)(F)(5), (VIII)(F)(7)

Claim 25

(VIII)(F)(3), (VIII)(F)(4), (VIII)(F)(5), (VIII)(F)(7)

Claim 26

(VIII)(F)(3), (VIII)(F)(5), (VIII)(F)(7), (VIII)(F)(8)

Claim 27

(VIII)(F)(3), (VIII)(F)(4), (VIII)(F)(5), (VIII)(F)(7), (VIII)(F)(8)

Claim 28

(VIII)(F)(3), (VIII)(F)(4), (VIII)(F)(5), (VIII)(F)(7), (VIII)(F)(8)

Claim 29

(VIII)(F)(3)

Claim 30

(VIII)(F)(3), (VIII)(F)(4)

Claim 31

(VIII)(F)(3), (VIII)(F)(4)

Claim 32

(VIII)(F)(1), (VIII)(F)(3), (VIII)(F)(4)

Claim 33

(VIII)(F)(3), (VIII)(F)(4), (VIII)(F)(5)

Claim 35

(VIII)(F)(3), (VIII)(F)(4)

Claim 36

(VIII)(F)(3), (VIII)(F)(4), (VIII)(F)(5)

Claim 37

(VIII)(F)(3), (VIII)(F)(4)

Claim 38

(VIII)(F)(3), (VIII)(F)(4), (VIII)(F)(5)

Claim 39

(VIII)(F)(3)

Claim 40

(VIII)(F)(3), (VIII)(F)(5)

Claim 41

(VIII)(F)(3)

Claim 42

(VIII)(F)(1), (VIII)(F)(3), (VIII)(F)(5)

Claim 43

(VIII)(F)(1), (VIII)(F)(3)

Claim 44

(VIII)(F)(3)

Claim 45

(VIII)(F)(3), (VIII)(F)(5)

Claim 46

(VIII)(F)(1), (VIII)(F)(3)

Claim 47

(VIII)(F)(3)

Claim 48

(VIII)(F)(2), (VIII)(F)(7)

Claim 49

(VIII)(F)(3), (VIII)(F)(7), (VIII)(F)(8)

Claim 50

(VIII)(F)(3), (VIII)(F)(7), (VIII)(F)(8)

Claim 51

(VIII)(F)(3)

Claim 52

(VIII)(F)(2), (VIII)(F)(3)

Claim 53

(VIII)(F)(2), (VIII)(F)(7)

Claim 54

(VIII)(F)(2), (VIII)(F)(7), (VIII)(F)(8)

Claim 55

(VIII)(F)(2), (VIII)(F)(3), (VIII)(F)(7)

Claim 56

(VIII)(F)(2), (VIII)(F)(7)

Claim 57

(VIII)(F)(2), (VIII)(F)(7)

Claim 58

(VIII)(F)(2), (VIII)(F)(7)

Claim 59

(VIII)(F)(2), (VIII)(F)(7)

Claim 65

(VIII)(F)(3), (VIII)(F)(5)

Claim 66

(VIII)(F)(1), (VIII)(F)(3)

G. The Failure of the Combination of the Cited References to Disclose or Suggest the Combination of Elements and Method Steps Recited in the Claims.

In order for different prior art references to be combined to reject a claim, the references have to disclose or suggest the combination of elements or method steps recited in the claim. ACS Hospitality Systems v. Montefiore Hospital, 732 F.2d 1572, 221, USPQ 929 (fed. Cir. 1984). As the Federal Circuit indicated in the ACS case at 732 F.2d 1577, 1579, 221 USPT 929, 933:

> "Obviousness cannot be established by combining the teachings of the prior art to produce the claimed invention absent some teaching or suggestion

As applicant indicates on page 13, lines 1-2:

Figure 5 shows how the stress in the nickel-vanadium layer 20 decreases with increases in the RF power applied."

This is not disclosed in the prior art including the Admitted Prior Art.

D. The Failure of Hong to Disclose What the Examiner States that Hong discloses

On page 9 of the Office Action dated 04/20/04, the Examiner states:

"However, Hong discloses a metal layer deposited on the surface of the wafer in a magnetron with no RF or with a RF in the magnetron and with a low flow rate (i.e. rate sufficient to deposit the metal layer) of molecules of an inert gas (i.e. argon) in the magnetron (see col. 1 lines 22-55 and col. 2 lines 1-39). Thus, any metal layer (i.e., chromium) can be deposited by the process of Hong, since any type of metal layer can not be ionized utilizing an environment with no RF bias or with a RF bias in the magnetron yielding a uniform deposition of metal."

First of all, the quotation above is incomprehensible. Applicant would appreciate it if the Examiner would clarify what he intended to state in the above quotation. Secondarily, col. 1, lines 22-55 and col. 2, lines 1-39 in Hong constitute background to the Hong invention. This background is so basic that it constitutes the equivalent of what would be taught in a beginner's class in the field of deposition techniques. Contrary to the position of the Examiner, Hong does not teach anything in columns 1 and 2 which would cause Hong to be applicable to any of the novel features of any one of claims 8, 13, 17, 24-27, 30-31, 33, 40, 42, and 65 against which Hong has been cited as prior art.

E. The Rejection of Claims 1 and 3-69 Because of the Alleged Failure of Applicant to Recite an Essential Step in the Claims

The Examiner has "rejected claims 1 and 3-69 under 35 U.S.C. 112, second paragraph as being incomplete for omitting essential steps, such omission amounting to a gap between the steps. See MPEP §2712.01. The omitted steps are, "a wafer disposed on a wafer land and a lens shield that is spaced from to (sic) the wafer land" since the lower powering step must include the combination of a wafer land and the lens shield in order to create argon ions forming microscopic roughness on the surface of the wafer."

Applicant is not required to specify the use of the wafer land and the lens shield to produce a wafer surface with a microscopic roughness. Instead, applicant has recited a proper method step involving the creation of a microscopic roughness on the surface of the wafer by providing ions of an inert gas with an insufficient energy to etch the surface of the wafer but with a sufficient energy to create the microscopic roughness on the surface of the wafer. Applicant respectfully submits that this recitation meets the requirements of MPEP §2172.01.

MPEP §2172.01 states the following:

> "A claim which omits matter disclosed to be essential to the invention as described in the specification or in any other statements of record may be rejected under 35 U.S.C. 112, first paragraph, as not enabling." (Underling supplied).

Applicant does not disclose in the specification that the use of the wafer land and the lens shield to create the microscopic roughness on the surface of the wafer is "essential". Therefore, MPEP §2172.01 is not applicable. This is particularly true since applicant recites in the claims that applicant provides the microscopic roughness on the surface of the wafer by providing ions of an inert gas on the surface of the wafer with an insufficient energy to etch the surface of the wafer

but with a sufficient energy to produce the microscopic roughness on the surface of the wafer. Applicant respectfully submits that this is a true method step and that it recites how applicant produces the microscopic roughness on the surface of the wafer.

The alleged method proposed by the Examiner is not actually a method step. The alleged method proposed by the Examiner recites apparatus limitations and, is proper for inclusion in apparatus claims. Only claims 44-58 in this application constitute apparatus claims.

Even if the Examiner's position under 35 U.S.C. § 112, second paragraph, should be sustained by the Board of Appeals, this would affect only a relatively few of the claims. This may be seen from the following:

1. Claims 4, 6, 7, 14-16, 20, 21, 23, 34, 60-64 and 67 have been allowed by the Examiner if rewritten in independent form including all of the limitations of the base claim and any intervening claims.
2. A number of the claims recite a wafer surface but do not recite that the wafer surface has a microscopic roughness. These include claims 5, 8, 11, 13, 17-18, 19, 48, 49, 50, 53, 54, 56, 57, 58 and 59. It is recognized that an applicant does not have to recite every limitation in every claim. Therefore, it is proper for applicant to recite the wafer surface without reciting that the wafer surface has a microscopic roughness. The claims are accordingly not affected by the requirement of the Examiner to recite the alleged step of "a wafer disposed on a wafer and a lens shield that is spaced from to (sic) the wafer land."
3. A number of the claims recite that the wafer surface has a microscopic roughness but do not recite how the microscopic roughness is formed.

These include claims 6, 9, 10, 12, 22, 24, 25, 26, 27, 28, 29, 30, 31, 33, 39, 40, 41, 44, 45, 47, 51, 52, 55 and 65. It is proper for applicant to recite that the wafer surface has a microscopic roughness without reciting how the microscopic roughness is produced. These claims are accordingly not affected by the requirement of the Examiner to recite the alleged step of a "wafer disposed on a wafer land and a lens shield that is spaced from to (sic) the wafer land."

F. The Distinctions of the Claims Over the Prior Art

As will be seen from the above, there are a number of distinctions between the recitations in applicant's claims and the prior art cited by the Examiner. These distinctions are summarized below. Each of the distinctions listed below is not disclosed in any of the references (including the Admitted Prior Art) cited by the Examiner to reject the claims, whether the references are used individually or in combination. The distinctions include the following:

1. Creating a microscopic roughness on a surface of a wafer to receive a deposition of chromium on the wafer surface by providing ions of an inert gas with an insufficient energy to etch the surface of the wafer but with a sufficient energy to create the microscopic roughness on the surface of the wafer. Then depositing a layer of chromium with a low intrinsic stress on the microscopically rough surface of the layer.

2. Depositing a layer of chromium with a low intrinsic tensile stress on a surface of a wafer. The surface of the wafer is not recited as being microscopically rough.

3. Depositing a layer of chromium on a microscopically rough surface of the wafer. The method of producing the microscopic roughness is not recited in the claim.

4. Providing a flow of an inert gas at a low rate on the wafer surface when the chromium layer is deposited on the surface of the wafer, thereby to minimize the presence of the inert gas in the chromium layer.

5. Depositing the chromium layer on the surface of the wafer in a magnetron with no RF bias in the magnetron and with a low flow rate of molecules of an inert gas in the magnetron.

6. Providing a chamber in which to perform the recited steps and passing molecules of an inert gas flow through the chamber in the order of three (3) to five (5) standard cubic centimeters per minute (3-5 sccm).

7. Depositing a layer of nickel vanadium on the chromium layer with a low intrinsic compressive stress.

8. Depositing a layer of nickel vanadium on the chromium layer with a low intrinsic compressive stress to neutralize the low intrinsic tensile stress of the chromium layer.

9. Depositing a nickel vanadium layer on the surface of the chromium layer with an RF bias power to produce a low intrinsic compressive stress in the nickel vanadium layer for neutralizing the low intrinsic tensile stress in the chromium layer.

Claims 1, 3, 5, 8-13, 17-19, 22, 24-33, 35-59, 65 and 66 have been rejected in view of the prior art cited by the Examiner. Each of these claims is allowable over the cited prior art because of particular distinctions specified above as paragraphs VII(F)(1-9). The distinctions causing each of the claims to be allowable over the cited references are specified below:

Claim 1

(VIII)(F)(1)

Claim 3

(VIII)(F)(1)

Claim 5

(VIII)(F)(2), (VIII)(F)(7)

Claim 8

(VIII)(F)(2), (VIII)(F)(3)

Claim 9

(VIII)(F)(3), (VIII)(F)(7), (VIII)(F)(8)

Claim 10

(VIII)(F)(3), (VIII)(F)(7), (VIII(F)(8)

Claim 11

(VIII)(F)(2)

Claim 12

(VIII)(F)(2), (VIII)(F)(3)

Claim 13

(VIII)(F)(2), (VIII)(F)(5)

Claim 17

(VIII)(F)(2), (VIII)(F)(7), (VII)(F)(8)

Claim 18

(VIII)(F)(2), (VIII)(F)(7), (VIII)(F)(8)

Claim 19

(VIII)(F)(2), (VIII)(F)(7), (VIII)(F)(8)

Claim 22

(VIII)(F)(3), (VIII)(F)(7)

Claim 24

(VIII)(F)(3), (VIII)(F)(5), (VIII)(F)(7)

Claim 25

(VIII)(F)(3), (VIII)(F)(4), (VIII)(F)(5), (VIII)(F)(7)

Claim 26

(VIII)(F)(3), (VIII)(F)(5), (VIII)(F)(7), (VIII)(F)(8)

Claim 27

(VIII)(F)(3), (VIII)(F)(4), (VIII)(F)(5), (VIII)(F)(7), (VIII)(F)(8)

Claim 28

(VIII)(F)(3), (VIII)(F)(4), (VIII)(F)(5), (VIII)(F)(7), (VIII)(F)(8)

Claim 29

(VIII)(F)(3)

Claim 30

(VIII)(F)(3), (VIII)(F)(4)

Claim 31

(VIII)(F)(3), (VIII)(F)(4)

Claim 32

(VIII)(F)(1), (VIII)(F)(3), (VIII)(F)(4)

Claim 33

(VIII)(F)(3), (VIII)(F)(4), (VIII)(F)(5)

Claim 35

(VIII)(F)(3), (VIII)(F)(4)

Claim 36

(VIII)(F)(3), (VIII)(F)(4), (VIII)(F)(5)

Claim 37

(VIII)(F)(3), (VIII)(F)(4)

Claim 38

(VIII)(F)(3), (VIII)(F)(4), (VIII)(F)(5)

Claim 39

(VIII)(F)(3)

Claim 40

(VIII)(F)(3), (VIII)(F)(5)

Claim 41

(VIII)(F)(3)

Claim 42

(VIII)(F)(1), (VIII)(F)(3), (VIII)(F)(5)

Claim 43

(VIII)(F)(1), (VIII)(F)(3)

Claim 44

(VIII)(F)(3)

Claim 45

(VIII)(F)(3), (VIII)(F)(5)

Claim 46

(VIII)(F)(1), (VIII)(F)(3)

Claim 47

(VIII)(F)(3)

Claim 48

(VIII)(F)(2), (VIII)(F)(7)

Claim 49

(VIII)(F)(3), (VIII)(F)(7), (VIII)(F)(8)

Claim 50

(VIII)(F)(3), (VIII)(F)(7), (VIII)(F)(8)

Claim 51

(VIII)(F)(3)

Claim 52

(VIII)(F)(2), (VIII)(F)(3)

Claim 53

(VIII)(F)(2), (VIII)(F)(7)

Claim 54

(VIII)(F)(2), (VIII)(F)(7), (VIII)(F)(8)

Claim 55

(VIII)(F)(2), (VIII)(F)(3), (VIII)(F)(7)

Claim 56

(VIII)(F)(2), (VIII)(F)(7)

Claim 57

(VIII)(F)(2), (VIII)(F)(7)

Claim 58

(VIII)(F)(2), (VIII)(F)(7)

Claim 59

(VIII)(F)(2), (VIII)(F)(7)

Claim 65

(VIII)(F)(3), (VIII)(F)(5)

Claim 66

(VIII)(F)(1), (VIII)(F)(3)

G. The Failure of the Combination of the Cited References to Disclose or Suggest the Combination of Elements and Method Steps Recited in the Claims.

In order for different prior art references to be combined to reject a claim, the references have to disclose or suggest the combination of elements or method steps recited in the claim. ACS Hospitality Systems v. Montefiore Hospital, 732 F.2d 1572, 221, USPQ 929 (fed. Cir. 1984). As the Federal Circuit indicated in the ACS case at 732 F.2d 1577, 1579, 221 USPT 929, 933:

> "Obviousness cannot be established by combining the teachings of the prior art to produce the claimed invention absent some teaching or suggestion

supporting the combination. Under Section 103, teaching of references can be combined only if there is some suggestion or incentive to do so."

Neither Akiyama, the Admitted Prior Art nor Hong cited by the Examine to reject the claims in this application discloses or suggests a number of the important features recited in the claims. The references cannot accordingly be combined to reject the claims.

IX. Conclusion

Claims 1, 3, 5, 8-13, 17-19, 22, 24-33, 35-59, 65 and 66 are allowable over the cited references whether the references are used individually or in combination.

Reconsideration and allowance of the application are respectfully requested.

10. Appendix

Claim 1: In a method of etching a surface of a wafer with a microscopic roughness to prepare the wafer surface for receiving a deposition of a material on the wafer surface, the steps of

removing a thin layer from the surface of the wafer to eliminate any impurities from the surface of the wafer, and

thereafter creating the microscopic roughness on the surface of the wafer to receive a deposition of the material on the surface by providing ions of an inert gas with an insufficient energy to etch the surface of the wafer but with a sufficient energy to create the microscopic roughness on the surface of the wafer.

Claim 2 (cancelled)

Claim 3: In a method as set forth in claim 2 wherein

the inert gas is argon.

Claim 4: In a method as set forth in claim 1 wherein

the wafer is disposed on a waferland and wherein

a layer of chromium is deposited on the waferland after the microscopic roughness has been produced on the surface of the wafer.

Claim 5: In a method of providing for an attachment of an electrical component to a wafer, the steps of:

removing a thin layer from the surface of the wafer,

thereafter depositing a chromium layer with a low intrinsic tensile stress on the cleaned surface of the wafer, and

thereafter depositing a layer of nickel vanadium with an intrinsic stress on the surface of the chromium layer to neutralize the low intrinsic tensile stress produced by the chromium layer.

Claim 6: In a method as set forth in claim 5wherein

a microscopic roughness is produced on the surface of the wafer after the thin layer of the wafer has been removed from the surface of the wafer and wherein

the chromium layer is thereafter deposited on the microscopically rough surface of the wafer and wherein

a low rate of flow of an inert gas is provided on the wafer layer when the chromium layer is deposited on the surface of the wafer thereby to minimize the presence of the inert gas in the chromium layer.

Claim 7: In a method as set forth in claim 5 wherein

a waferland is disposed in an abutting relationship with the wafer and wherein

a layer of chromium is deposited on the surface of the waferland before etching the surface of the wafer.

Claim 8: In a method as set forth in claim 5 wherein

the chromium layer is deposited on the surface of the wafer to produce an intrinsic tensile stress in the chromium layer and wherein

the nickel vanadium layer is deposited on the surface of the chromium layer with an RF bias power to produce an intrinsic compressive stress in the nickel vanadium layer.

Claim 9: In a method as set forth in claim 5 wherein

the chromium is deposited in a layer on the microscopically rough surface of the wafer to produce an intrinsic tensile stress with a low stress value in the chromium layer and wherein

the nickel vanadium layer is deposited on the surface of the chromium layer to produce a low intrinsic compressive stress with a value to neutralize the low intrinsic tensile stress in the chromium layer.

Claim 10: In a method as set forth in claim 7 wherein

the chromium is deposited in a layer on the microscopically rough surface of the wafer in an intrinsic tensile stress with a low stress value and wherein

the layer of the nickel vanadium is deposited on the surface of the chromium in an intrinsic compressive stress with a low stress value substantially neutralizing the low stress value of the intrinsic tensile stress of the chromium layer.

Claim 11: In a method of providing for an attachment of an electrical component to a wafer, the steps of:

removing a thin layer from the surface of the wafer, and

depositing a chromium layer with a low intrinsic tensile stress on the surface of the wafer after the removal of the thin layer from the surface of the wafer.

Claim 12: In a method as set forth in claim 11 wherein

the surface of the wafer is provided with a microscopic roughness after the thin layer has been removed from the surface of the wafer and wherein

the chromium layer is deposited on the microscopically rough surface of the wafer in an intrinsic tensile stress with a low stress value.

Claim 13: In a method as set forth in claim 11 wherein

the chromium layer is deposited on the surface of the wafer in a magnetron with no RF bias in the magnetron and with a low flow rate of molecules of an inert gas in the magnetron.

Claim 14: In a method as set forth in claim 11 wherein

a chamber is provided in which to perform the recited steps and wherein molecules of an inert gas flow through the chamber in an order of three (3) to five (5) standard cubic centimeters per minute (3-5 sccm).

Claim 15: In a method as set forth in claim 12 wherein

a chamber is provided in which to perform the recited steps and wherein

a waferland is disposed in the chamber to support the wafer and wherein a layer of chromium is deposited on the waferland before the chromium layer is deposited on the surface of the wafer.

Claim 16: In a method as set forth in claim 11 wherein

a waferland and a chamber are provided and the wafer and the waferland are disposed in the chamber and wherein

the chromium layer is deposited on the surface of the wafer in the chamber with no RF bias on the waferland in the chamber and with a low flow rate of molecules of an inert gas in the chamber,

the inert gas is argon and the flow rate of the molecules of the inert gas in the chamber is in the order of three (3) to five (5) standard cubic centimeters per minute (3-5 sccm).

Claim 17: In a method of providing for an attachment of an electrical component or sub-assembly to a wafer, the steps of:

removing a thin layer from the surface of the wafer,

depositing a layer of chromium on the surface of the wafer with a low intrinsic tensile stress, and

depositing a nickel vanadium layer on the surface of the chromium layer with an RF bias power to produce a low intrinsic compressive stress in the nickel vanadium layer for neutralizing the low intrinsic tensile stress in the chromium layer.

Claim 18: In a method as set forth in claim 17 wherein

a layer of metal selected from the group consisting of gold, silver and copper is deposited on the surface of the layer of nickel vanadium and wherein

the nickel vanadium layer has a low intrinsic compressive stress to neutralize the low intrinsic tensile stress in the chromium layer and any stress in the metal layer selected from the group consisting of gold, silver and copper.

Claim 19: In a method as set forth in claim 18 wherein

the electrical component is soldered to the layer of the metal selected from the group consisting of gold, silver and copper.

Claim 20. In a method as set forth in claim 18 wherein

the wafer is disposed on a waferland and wherein

a layer of chromium is deposited on the waferland before the thin layer is removed from the surface of the wafer and wherein

the electrical component is soldered to the layer of the metal selected from the group consisting of gold, silver and copper.

Claim 21: In a method as set forth in claim 20 wherein

a lens shield is disposed in a spaced relationship to the waferland and the lens shield is grounded and wherein

the RF bias power for the deposition of the layer of nickel vanadium is provided between the waferland and the grounded lens shield.

Claim 22: In a method of providing for an attachment of an electrical component to a wafer, the steps of:

removing a thin layer from the surface of the wafer,

thereafter providing the surface of the wafer with a microscopic roughness,

thereafter depositing a layer of chromium on the microscopically rough surface of the wafer with a low intrinsic tensile stress, and

thereafter depositing a layer of nickel vanadium on the surface of the wafer with a low intrinsic compressive stress.

Claim 23: In a method as set forth in claim 21 wherein

a layer of a metal selected from a group consisting of gold, nickel and copper is deposited on the surface of the nickel vanadium layer and wherein

a component is soldered to the layer of the metal selected from the group consisting of copper, gold and silver.

Claim 24: In a method as set forth in claim 23 wherein

the layer of the chromium is deposited on the microscopically rough surface of the wafer with no RF bias.

Claim 25: In a method as set forth in claim 22 wherein

the layer of chromium is deposited on the microscopically rough surface of the wafer at a low rate of the flow of an inert gas.

Claim 26: In a method as set forth in claim 24 wherein

the layer of chromium is deposited on the microscopically rough surface of the wafer at a low rate of flow of an inert gas and wherein

an RF bias power is applied during the deposition of the nickel vanadium layer on the chromium layer to produce the low intrinsic compressive stress in the nickel vanadium layer.

Claim 27: In a method as set forth in claim 21 wherein

the layer of the chromium is deposited on the microscopically rough surface of the wafer with no RF bias and wherein

the layer of chromium is deposited on the microscopically rough surface of the wafer at a low rate of flow of an inert gas and wherein

an RF bias power is applied during the deposition of the nickel vanadium layer on the chromium layer to produce the low intrinsic compressive stress in the nickel vanadium layer.

Claim 28: In a method as set forth in claim 27 wherein

a layer of a metal selected from a group consisting of gold, nickel and copper is deposited on the surface of the nickel vanadium layer and wherein

the component is soldered to the layer of the metal selected from the group consisting of copper, gold and silver.

Claim 29: In a method of providing a deposition on a surface of a wafer, the steps of:

removing a thin layer from the surface of the wafer to eliminate impurities from the surface of the wafer,

creating a microscopic roughness on the surface of the wafer, and

depositing a chromium layer with a low intrinsic tensile stress on the microscopically rough surface of the wafer.

Claim 30: In a method as set forth in claim 29 wherein

the chromium layer is deposited on the microscopically rough surface of the wafer in a chamber and wherein

an inert gas having a low flow rate is passed through the chamber with no RF bias on the wafer, when the chromium layer is deposited on the microscopically rough surface of the wafer, to prevent molecules of the inert gas from being entrapped in the chromium layer.

Claim 31: In a method as set forth in claim 30 wherein

the inert gas is argon.

Claim 32: In a method as set forth in claim 30 wherein

the microscopic roughness is produced on the surface of the wafer by providing the molecules of the inert gas with an insufficient energy to etch the surface of the wafer but with a sufficient energy to create the microscopic roughness on the surface of the wafer.

Claim 33: In a method as set forth in claim 29 wherein

no RF bias is provided when the chromium layer is deposited on the surface of the wafer and wherein

the chromium layer is deposited on the microscopically rough surface of the wafer in a chamber and wherein

an inert gas having a low flow rate is passed through the chamber, when the chromium layer is deposited on the microscopically rough surface of the wafer, to prevent the inert gas from being entrapped in the chromium layer and wherein

the inert gas is argon.

Claim 34: In a method as set forth in 31 wherein

the wafer is disposed on a waferland and wherein

a layer of chromium is deposited on the waferland, before etching the wafer surface, to prevent the layer of chromium deposited on the wafer from being contaminated by the material from the waferland.

Claim 35: In a method of preparing a wafer surface for receiving an electronic component, the steps of:

removing a thin layer from the surface of the wafer,

thereafter creating a microscopic roughness on the surface of the wafer by providing ions of an inert gas with an insufficient energy to etch the surface of the wafer but with a sufficient energy to create the microscopic roughness on the surface of the wafer, and

thereafter depositing a chromium layer on the microscopically rough surface of the wafer in a chamber in which a minimal amount of an inert gas is passed through the chamber during the deposition to prevent molecules of the inert gas from being entrapped in the chromium layer.

Claim 36: In a method as set forth in claim 35 wherein

no wafer bias is produced on the wafer when the chromium layer is deposited on the surface of the wafer.

Claim 37: In a method as set forth in claim 35 wherein

the chromium layer is deposited on the surface of the wafer under tension with a low amount of stress.

Claim 38: In a method as set forth in claim 36 wherein

the chromium layer is deposited on the surface of the wafer with a low amount of intrinsic tensile stress.

Claim 39: In a method of providing a deposition on a surface of a wafer for receiving an electronic component on the wafer surface, the steps of:

removing a thin layer from the surface of the wafer,

creating a microscopic roughness on the surface of the wafer, and

atomically bonding a chromium layer to the microscopically rough surface on the wafer.

Claim 40: In a method as set forth in claim 39 wherein

the chromium layer is deposited on the microscopically rough surface of the wafer with no RF bias.

Claim 41: In a method as set forth in claim 39, the step of:

providing a low intrinsic tensile stress in the chromium layer.

Claim 42: In a method as set forth in claim 39 wherein

the microscopic roughness on the surface of the wafer is provided by disposing the wafer in a chamber and by passing ions of an inert gas through the chamber with insufficient energy to etch the surface of the wafer but with sufficient energy to produce the microscopic roughness on the surface of the wafer.

Claim 43: In a method as set forth in claim 40 wherein

providing an intrinsic tensile stress with a low value in the chromium layer and wherein

the microscopic roughness on the surface of the wafer is provided by disposing the wafer in a chamber and by passing ions of an inert gas through the chamber with insufficient energy to etch the surface of the wafer but with sufficient energy to produce the microscopic roughness on the surface of the wafer.

Claim 44: In combination for performing electrical functions,

a wafer having a clean surface with a microscopic roughness, and

a layer of chromium deposited on the microscopically rough surface of the wafer with a low intrinsic tensile stress in the chromium layer.

Claim 45: In a combination as set forth in claim 44 wherein

the chromium layer is deposited on the microscopically rough surface of the wafer with a low intrinsic tensile stress at a rate of flow of an inert gas in the order of 3-5 SCCM.

Claim 46: In a combination as set forth in claim 44 wherein

the microscopic roughness is provided on the surface of the wafer by ions of an inert gas with an insufficient energy to etch the surface of the wafer but with sufficient energy to produce the microscopic roughness on the surface of the wafer.

Claim 47: In a combination as set forth in claim 44 wherein

an atomic bonding is produced between the chromium in the chromium layer and the microscopically rough surface of the wafer.

Claim 48: In combination for performing electrical functions,

a wafer,

a chromium layer deposited on the wafer with a low intrinsic tensile stress, and

a layer of nickel vanadium deposited on the chromium layer in firmly adhered relationship to the chromium layer with a low intrinsic compressive stress.

Claim 49: In a combination as set forth in claim 48,

the chromium layer being under the low intrinsic tensile stress and the nickel vanadium layer being under the low intrinsic compressive stress to neutralize the low intrinsic tensile stress of the chromium layer.

Claim 50: In a combination as set forth in claim 48,

the chromium in the chromium layer having the low intrinsic tensile stress for bonding to the microscopically rough wafer surface,

the chromium in the chromium layer having an atomic bonding with the microscopically rough surface on the wafer.

Claim 51: In combination for performing electrical functions,

a wafer having a clean surface with a microscopic roughness, and

a chromium layer deposited on the microscopically rough surface of the wafer and atomically bonded to the microscopically rough wafer surface.

Claim 52: In a combination as set forth in claim 51,

the chromium layer having a low intrinsic tensile stress for bonding to the microscopically rough wafer surface.

Claim 53: In combination for performing electrical functions,

a wafer having a clean surface,

a chromium layer disposed on the clean surface of the wafer with an intrinsic tensile stress, and

a nickel vanadium layer deposited on the chromium layer with a low intrinsic compressive stress.

Claim 54: In a combination as set forth in claim 53 wherein

the low intrinsic compressive stress of the nickel vanadium layer substantially neutralizes the low intrinsic tensile stress of the chromium layer.

Claim 55: In a combination as set forth in claim 53 wherein

the clean surface of the wafer has a microscopic roughness and wherein

the chromium in the chromium layer is atomically bonded to the microscopically rough surface of the wafer.

Claim 56: In a combination as set forth in claim 52,

a layer of a metal selected from the group consisting of copper, gold and silver and disposed on the nickel vanadium layer with a low intrinsic tensile stress.

Claim 57: In a combination as set forth in claim 53 wherein

a layer of a metal selected from the group consisting of copper, gold and silver is deposited on the nickel vanadium layer and wherein

the nickel vanadium layer substantially neutralizes any intrinsic stress in the metal layer selected from the group consisting of copper, gold and silver.

Claim 58: In a combination as set forth in claim 53 wherein

an electrical component is soldered to the layer of the metal selected from the group consisting of copper, gold and silver.

Claim 59: In a method of etching a surface of a wafer with a microscopic roughness, the steps of:

providing a flow of an inert gas in the order of forty (40) to fifty (50) standard cubic centimeters per minute through a chamber containing the wafer and at a relatively high gas pressure in the order of 4-6 $10^{-3}$ Torrs to remove a thin layer from the surface of the wafer,

thereafter providing a flow of an inert gas through the chamber at a flow rate of approximately forty (40) to fifty (50) standard cubic centimeters per minute and a

power in the order of six hundred watts (600 W) to twelve hundred watts (1200 W) to remove impurities from the surface of the wafer and provide an anatomically rough surface,

disposing the wafer on a waferland, and

then providing a flow of an inert gas at a rate of approximately 40-50 standard cubic centimeters per minute through the chamber at a low power in the order of fifty watts (50 W) to one hundred watts (100 W) to provide the surface of the wafer with the microscopic roughness.

Claim 60: In a method as set forth in claim 59 wherein

the power applied in the chamber to remove the impurities from the surface of the wafer is in the order of 600-1200 watts for approximately thirty (30) seconds and wherein

the flow of the inert gas through the chamber to provide the surface of the wafer with the microscopic roughness occurs for a period of approximately sixty (60) seconds.

Claim 61: In a method as set forth in claim 59 wherein

a layer of chromium is deposited on the microscopically rough surface of the wafer without any RF bias and at a low flow rate of the inert gas.

Claim 62: In a method as set forth in claim 59 wherein

a layer of nickel vanadium is deposited on the surface of the chromium layer with an RF bias power of approximately 300 watts and with a flow rate of argon of approximately 5 sccm.

Claim 63: In a method as set forth in claim 60 wherein

a layer of chromium is deposited on the surface of the waferland before the surface of the wafer is etched.

Claim 64: In a method as set forth in claim 60 wherein

the nickel vanadium layer is deposited on the chromium layer with a power of approximately six thousand watts (6000 W), with a flow rate of argon of approximately five (5) sccm and with RF power of approximately three hundred (300) watts.

Claim 65: In a method as set forth in claim 29 wherein

the chromium layer is deposited with a low intrinsic tensile stress on the microscopically rough surface by providing the layer with no RF bias.

Claim 66: In a method as set forth in claim 29 wherein

the microscopic roughness is created on the surface of the wafer by providing ions of an inert gas on the surface of the wafer with an insufficient energy to etch the surface of the wafer but with a sufficient energy to create the microscopic roughness on the surface of the wafer.

Claim 67: In a method as set forth in claim 1 wherein

the inert gas is argon and wherein

the wafer is disposed on a waferland and wherein

a layer of chromium is deposited on the waferland after the microscopic roughness has been produced on a the surface of the wafer.

Claim 68: In a method as set forth in claim 22 wherein

the microscopic roughness on the surface of the layer is created by providing ions of an inert gas on the surface of the wafer with an insufficient energy to etch the surface of the wafer but with a coefficient energy to create the microscopic roughness on the surface of the wafer.

Claim 69: In a method as set forth in claim 39 wherein

the microscopic roughness is created on the surface of the wafer by providing ions of an inert gas on the surface of the wafer with an

insufficient energy to etch the surface of the wafer but a sufficient energy to create the microscopic roughness on the surface of the wafer.

Respectfully submitted,

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